REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated September 9, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-5 and 18-26 are under consideration in this application. Claims 1, 4-5, and 23 are being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim Applicants' invention. New claims 25-26 are being added to recite other embodiments described in the specification.

All the amendments to the claims are supported by the specification. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1-5 and 18-24 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,212,777 to Gove et al. (hereinafter "Gove") in view of U.S. Patent No. 5,978,592 to Wise (hereinafter "Wise"). This rejection has been carefully considered, but is most respectfully traversed.

The semiconductor integrated circuit 1 on a semiconductor chip of the invention (for example, the embodiment depicted in Figs. 1-2 and 10) 1 comprises: a central processing unit 2 conducting a single instruction multiple data (SIMD) command; a single instruction multiple data (SIMD) unit 3 controlled by the central processing unit 2 and including a plurality of operation units conducting a concurrent operation for a plurality of data items respectively fetched therein in accordance with interpretation result of said SIMD command by said central processing unit; a data buffer 9 connectible to said SIMD unit 3; and a data transfer control unit 5 for controlling transfer of data for said data buffer 9. The data transfer control unit 5 controls the transfer of data for a subsequent operation of the STMD unit 3 to said data buffer 9 ***from a memory 17*** (outside of the data buffer 9) *in concurrence with* the current operation of the SIMD unit 3 for a plurality of data items read ***from said data buffer 9***

(to internal components, such as registers 41, 42, p. 26, line 22).

In concurrence with the current processing by the SIMD operator 40 of the SIMD unit 3, the data for the subsequent processing is externally transferred from the memory 17 to the data buffer 9. "*The period of time used for the actual DMA transfer becomes invisible in the processing time. As a result, SIMD operation performance of the data processor 1 is increased. The SIMD operator 40 is always in a state in which necessary data with the code extension is prepared for operation.*" This increases the operational efficiency of the SIMD operator 40 (Fig. 10; [0073] of US. Pat. App. Pub. No. 20020184471), i.e., the operation of the SIMD unit 3 is not interrupted by the internal transfer of the data to the data buffer 9 ([0013] to [0017]). Therefore, the SIMD unit 3 continuously and efficiently conducts the operation. Furthermore, the SIMD unit 3 is controlled by the central processing unit 2 that conducts a single instruction multiple data (SIMD) command.

The invention recited in claim 25 is directed to the semiconductor integrated circuit 1 on a semiconductor chip of claim 1. The data transfer control unit 5 includes first data aligners 61 and bit extension units 25. The data aligners 61 prepares data in an arbitrary pixel unit necessary for the SIMD operation for the data transfer to increase executing performance of the SIMD operation. The bit extension units 25 carries out necessary code extension in the data transfer to further increase the SIMD operation efficiency. The data buffer 9 has a first port (e.g., 9B in Figs. 2 & 15, 9A and 53 in Figs. 11 & 14) coupled to the operation units in the SIMD unit and providing the first data items to the operation units in the SIMD unit under control of the CPU 2, and a second port (e.g., 9A in Figs. 2 & 15, 9A and 53 in Figs. 11 & 14).

Applicants respectfully contend that Gove fails to teach or suggest such a "data transfer control unit 5 controls the transfer of data for a subsequent operation of the STMD unit 3 to said data buffer 9 from a memory 17 in concurrence with the current operation of said SIMD unit 3 for a plurality of data items read from said data buffer 9" as in the invention

As admitted by the Examiner (p. 3, last paragraph of the outstanding Office Action), Gove did not teach such a feature of the invention. Gove only arranges a multiprocessor system as an image and graphics processor. The processor is structured with "n" number of individual processors PP0-PPj all having communication links to "m" number of memories M0-Mj without restriction. A crossbar switch 20 serves to establish the processor memory links. The entire image processor, including the individual processors PP0-PPj, the crossbar switch 20 and the memories 10 are contained on a single silicon chip (Fig. 1). Each processor

PP0-PPj can operate to execute the same instruction at the same time (StMD mode) or different instructions at the same time (MIND mode). See Abstract. These "*processors [100-104] are arranged to operate independently from each other from instructions executed on a cycle-by-cycle basis* (col. 2, lines 5-8)" thereby "*changing at least some of the processors from the group of processors from operation in the SIMD operating mode (i.e., executing the same instruction at the same time) to operation in the MIMD operational mode (i.e., executing different instructions at the same time) where each processor of the group operates from separate instructions provided by separate instruction memories* (col. 3, lines 15-20)".

Gove's transfer processor 11 (the alleged data transfer control unit 5) transfers data from the external memory 15 (Fig. 2) via a bus 21 (col. 5, lines 35-48) as well as transfer data from its internal memory 10 (the alleged data buffer 9) via the crossbar switch 20 to the internal memory 10, and Gove's internal memory 10 also transfers data to the master processor 12 (arguable equivalent of the SIMD unit 3) via the crossbar switch 20. However, Gove's transfer processor 11 (col. 12, lines 31-56) does not concurrently (1) transfer data for a *subsequent* operation of the master processor 12 from outside of chip to internal memory 10, and (2) transfer data for the *current* operation of the master processor 12 for a plurality of data items read from the internal memory *10* (to other internal components).

Wise was relied upon by the Examiner to compensate for Gove's deficiencies. However, one skilled in the art would not be motivated to look into Wise's data flow architecture for inspiration for improving Gove's multi-processor single-switch architecture. Gove's crossbars are controlled by a crossbar switch 20 (Figs. 1-2) which is provided between SIMD processors 100-103 and local memories MO-Mj in a memory 10 (the alleged data buffer 9) to change the connections between the SIMD processors 100-103 and the local memories M0-Mj. Gove's multi-processor single-switch architecture is incompatible with Wise's data flow architecture (e.g., Fig. 1 "*illustrates six cycles of a six-stage pipeline for different combinations of two internal control signals*" col. 7, lines 16-17), i.e., a data pipeline system which has one or more of the five characteristics, such as "elastic", etc. Although not shown in FIG. 1, there are data lines, either single lines or several parallel lines, which form a data bus that also lead into and out of each pipeline stage. Data is transferred into, out of, and between the stages of the pipeline over the data lines (col. 13, lines 25-62).

The Examiner's reliance upon the "common knowledge and common sense" of one skilled in the art for the motivation for combining the teachings Wise with Gove did not fulfill the agency's obligation to cite references to support its conclusions. Instead, the

Examiner must provide the specific teaching of allegations of the combination on the record to allow accountability.

> *It is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. Zurko, 258 F.3d at 1385, 59 USPQ2d at 1697 ("[T]he Board cannot simply reach conclusions based on its own understanding or experience-or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings."). While the court explained that, "as an administrative tribunal the Board clearly has expertise in the subject matter over which it exercises jurisdiction," it made clear that such "expertise may provide sufficient support for conclusions [only] as to peripheral issues." Id. at 1385-86, 59 USPQ2d at 1697. As the court held in Zurko, an assessment of basic knowledge and common sense that is not based on any evidence in the record lacks substantial evidence support. Id. at 1385, 59 USPQ2d at 1697. See also In re Lee, 277 F.3d 1338, 1344-45, 61 USPQ2d 1430, 1434-35 (Fed. Cir. 2002) (In reversing the Board's decision, the court stated "'common knowledge and common sense' on which the Board relied in rejecting Lee's application are not the specialized knowledge and expertise contemplated by the Administrative Procedure Act. Conclusory statements such as those here provided do not fulfill the agency's obligation..The board cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth the rationale on which it relies."). MPEP2144.03*

Such an obligation to provide specific teaching(s) also applies to other existing or future obviousness rejections.

Applicants respectfully contend that one skilled in the art will not be motivated to provide Wise's double-buffer mechanism into Gove's multi-processor single-switch architecture, except by using Applicants' system as a blueprint. Wise's double-buffer mechanism simply does not constitute common knowledge in the art of SIMD processing.

"It is never appropriate to rely solely on "common knowledge" in the art without evidentiary support in the record, as the principal evidence upon which a rejection was based. Zurko, 258 F.3d at 1385, 59 USPQ2d at 1697 ("[T]he Board cannot simply reach conclusions based on its own understanding or experience-or on its assessment of what would be basic

knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings."). While the court explained that, "as an administrative tribunal the Board clearly has expertise in the subject matter over which it exercises jurisdiction," it made clear that such "expertise may provide sufficient support for conclusions [only] as to peripheral issues." Id. at 1385-86, 59 USPQ2d at 1697. As the court held in Zurko, an assessment of basic knowledge and common sense that is not based on any evidence in the record lacks substantial evidence support. Id. at 1385, 59 USPQ2d at 1697. See also In re Lee, 277 F.3d 1338, 1344-45, 61 USPQ2d 1430, 1434-35 (Fed. Cir. 2002) (In reversing the Board's decision, the court stated " 'common knowledge and common sense' on which the Board relied in rejecting Lee's application are not the specialized knowledge and expertise contemplated by the Administrative Procedure Act. Conclusory statements such as those here provided do not fulfill the agency's obligation.. The board cannot rely on conclusory statements when dealing with particular combinations of prior art and specific claims, but must set forth the rationale on which it relies."). " As such the Examiner shall provide "some concrete evidence in the record in support of" factual assertion to rely solely on "common knowledge" in the art as the principal evidence.

Applicants will further contend that the combination of references used by the Examiner merely consists of selecting bits and pieces from each reference, and then combining those bits and pieces using knowledge or hindsight gleaned from the disclosure of the present invention as a guide to support the combination. The well established rule of law is that each prior art reference must be evaluated as an entirety, and that all of the prior art must be considered as a whole," *Panduit Corp. v. Dennison Mfg. Co.*, 227 USPQ 337, 344 (Fed. Cir. 1985). See *Para-Ordinance Mfg, Inc. v. SGS Importers Intl.*, Inc., 73 F.3d 1085, 37 USPQ2d 1237 (Fed. Cir. 1995) ("Obviousness may not be established using hindsight or in view of the teachings or suggestions of the inventor.").

Applicants contend that neither Gove, Wise, nor any other cited reference teaches or suggests each and every feature of the present invention as disclosed in the independent claims 1 and 25. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the

present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicants respectfully contend that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicants' undersigned representative at the address and phone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive, Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

March 8, 2006

SPF/JCM/JT